

1 General description

The PF8250 is a power management integrated circuit (PMIC) designed for high performance i.MX 8 and S32V based applications. It features seven high efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 2 qualified.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states.

Note: Electrical characteristics are maintained in the PF8150_PF8250 data sheet

2 Features and benefits

- Up to seven high efficiency buck converters
- Four linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog monitoring
- Independent OV/UV monitoring circuits
- One-time programmable device configuration
- 3.4 MHz I2C communication interface
- 56-pin 8 x 8 QFN package
- AEC-Q100 grade 2 qualified
- Safety mechanisms to fit ASIL B applications

3 Applications

- Automotive Infotainment
- High-end consumer and industrial



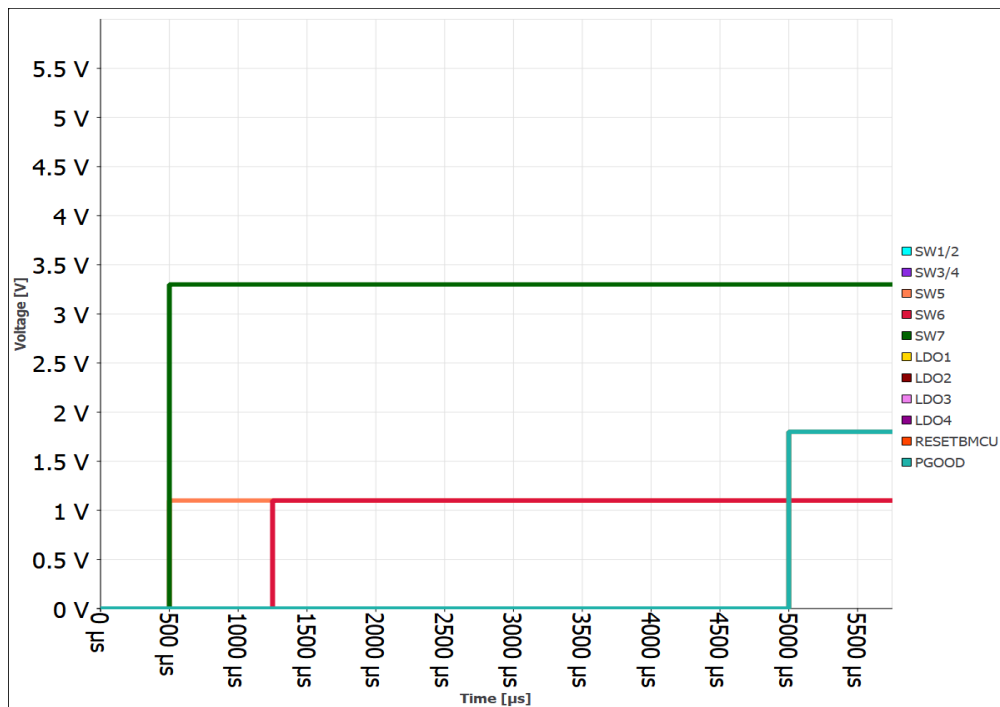
4 Ordering information

Table 1. Ordering information

Type number ^[1]	Package		
	Name	Description	Version
MC33PF8250DBTS	HVQFN56	HVQFN56, thermal enhanced very thin quad flat package, no leads, 56 terminals, 0.1 mm dimble wettable flank, 0.5 mm pitch, 8 mm x 8 mm x 0.9 mm body	SOT684-29(D)

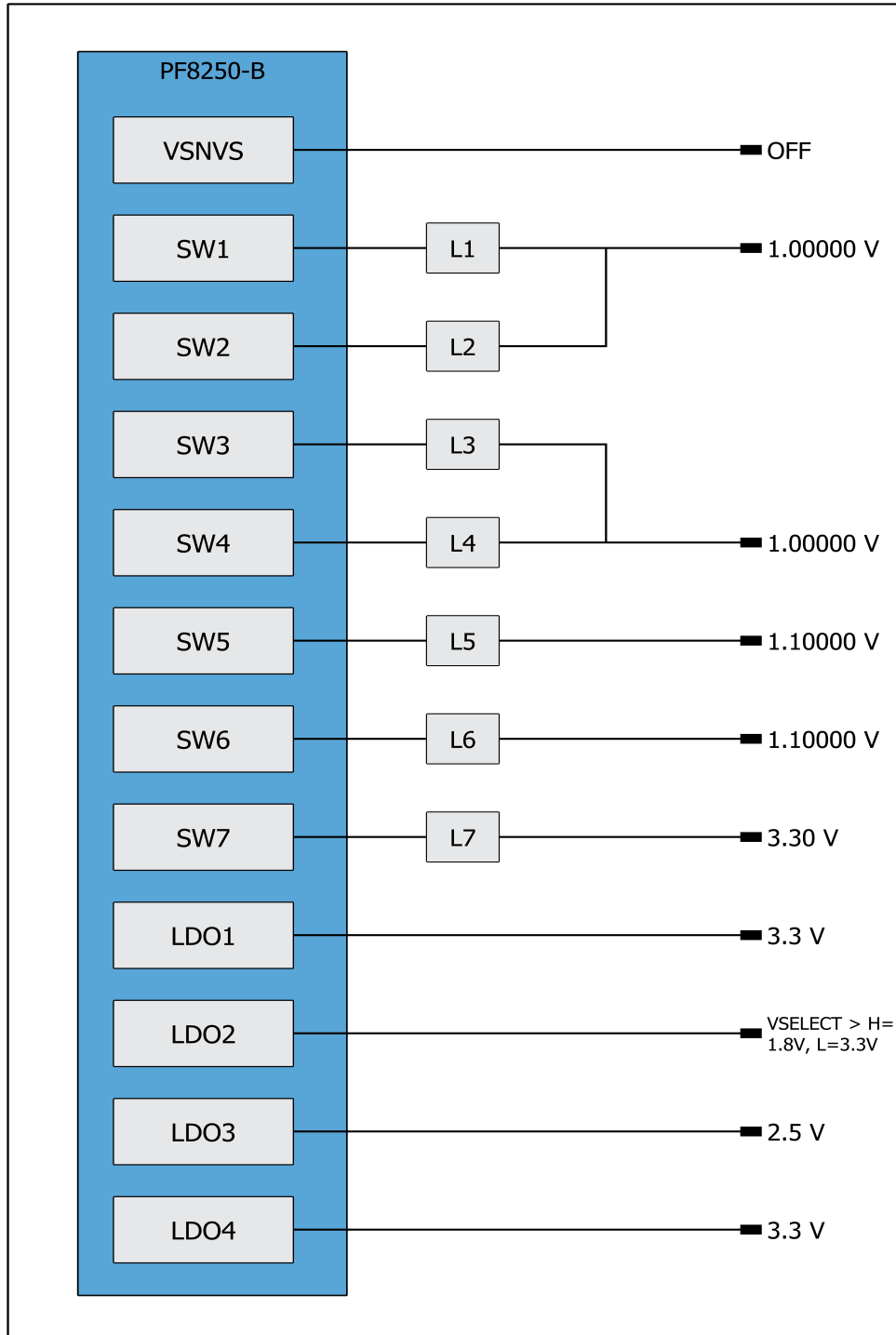
[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

6 Hardware configuration diagram



7 OTP configuration

See PF8150_PF8250 data sheet for parametric details. The OTP configuration summary for DB (sequence ID) is provided in Tables below.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
System configuration	I2C Address	0x09
	I2C CRC	Enabled
	I2C Secure Write	Secure Write Disabled
	VIN OVLO Monitor	VIN_OVLO Enabled
	VIN OVLO Debounce	100µs
	VIN OVLO Shutdown	VIN_OVLO Shutdown Disabled
	Maximum Fault Count	Disabled
	Fault Timer	DISABLED
	Fail Safe State	FailSafe Disabled
	Fail-safe Maximum Count	15
	Fail-safe OK Timer	60 min
Watchdog monitoring	WDI Mode	Hard WD Reset
	WDI Polarity	WD event detected on rising edge
	WDI In Standby	WDI event Disabled in Standby
	WD Counter	WD Timer Disabled
	WD Counter In Standby	WD Timer Disabled in Standby
	WD Clear Window	Clear within 100% of window
	Maximum Time Out Steps	7
	WD Duration	1024 ms
	Maximum WD Event	15

Configuration report for PF8250-B OTP program ID: DB rev A

Clock management	Switching Frequency	2.5 MHz
	SYNCIN Range	2000KHz to 3000KHz
	SYNCIN Operation	Disabled
	SYNCOUT Operation	Disabled
	Frequency Spread Spectrum	Frequency Spread Spectrum Disabled
	FSS Range	FSS Range set to 5%
COINCELL Control	Coin Cell Charging Voltage	3.0 V

Table 3. I/Os configuration

Functional block	Feature	OTP selection
I/O Configuration	PWRON Mode	Level Sensitive
	PWRON Debounce	32 msec
	PWRON Reset Mode	Shut down >TRESET
	TRESET Delay	2 sec
	STANDBY Polarity	STANDBY Active High
	PGOOD Pin Mode	PGOOD Indicator
	OV/UV Check On Power Up	PGOOD monitoring on PWRUP disabled
	EWARN Time	0.1ms
	XFAILB Operation	XFAILB Operation Enabled
	FSOB Soft Fault Event	Event does not assert FSOB
	FSOB Hard Fault Event	Event does not assert FSOB
	FSOB WDI Event	Event does not assert FSOB
	FSOB WDC Event	Event does not assert FSOB
	FSOB Operating Mode	Active Safe State Disabled

Configuration report for PF8250-B OTP program ID: DB rev A

Table 4. Sequencer configuration

Functional block	Feature	OTP selection
SW configurations	SW1 Multiphase Selector	SW1/2 Dual Phase
	SW4 Multiphase Selector	SW3/4 Dual Phase
	SW5 Multiphase Selector	SW5/6 Single Phase
	Default SW Operation	SW Regulators Default in PWM mode
	SW6 VTT Mode	VTT Mode Disabled
	VTT Discharge Mode	VTT Output Disable in HI-Z
	Bandgap Monitor Reaction	Bandgap comparator enabled
Power-up sequence	Sequencer Time Base	250 μ s
	SW1 Sequence	OFF
	SW2 Sequence	OFF
	SW3 Sequence	OFF
	SW4 Sequence	OFF
	SW5 Sequence	Slot 2
	SW6 Sequence	Slot 5
	SW7 Sequence	Slot 2
	LDO1 Sequence	OFF
	LDO2 Sequence	OFF
	LDO3 Sequence	OFF
	LDO4 Sequence	OFF
	RESETBMCU Sequence	Slot 20
	PGOOD Sequence	Slot 20
Power down sequence	Power Down Mode	Mirror power up sequence

Configuration report for PF8250-B OTP program ID: DB rev A

	SW1 Power Down Group	Group 4 (1st)
	SW2 Power Down Group	Group 4 (1st)
	SW3 Power Down Group	Group 4 (1st)
	SW4 Power Down Group	Group 4 (1st)
	SW5 Power Down Group	Group 4 (1st)
	SW6 Power Down Group	Group 4 (1st)
	SW7 Power Down Group	Group 4 (1st)
	LDO1 Power Down Group	Group 4 (1st)
	LDO2 Power Down Group	Group 4 (1st)
	LDO3 Power Down Group	Group 4 (1st)
	LDO4 Power Down Group	Group 4 (1st)
	RESETBMCU Power Down Group	Group 4 (1st)
	PGOOD Power Down Group	Group 4 (1st)
Power Down Delays	Group 1 Power Down Delay	120 μ s
	Group 2 Power Down Delay	120 μ s
	Group 3 Power Down Delay	120 μ s
	Group 4 Power Down Delay	120 μ s
	RESETBMCU Group Delay	10 μ s
	Power Down Delay	5 ms

Table 5. Switching regulators

Functional block	Feature	OTP selection
SW1	SW1 Output Voltage	1.00000 V
	SW1 DVS Ramp	7.813/5.208 mV/ μ s
	SW1 UV Threshold	93%

Configuration report for PF8250-B OTP program ID: DB rev A

	SW1 OV Threshold	107%
	SW1 Current Limit	4.5 A
	SW1 Inductor	1 μ H
	SW1 Phase	0°
	SW1 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW1 WD Bypass	Regulator reacts upon a Watchdog
	SW1 OV Bypass	OV Protect Enabled
	SW1 UV Bypass	UV Protect Enabled
	SW1 ILIM Bypass	ILIM Fault Bypassed
SW2	SW2 Output Voltage	1.00000 V
	SW2 DVS Ramp	7.813/5.208 mV/ μ s
	SW2 UV Threshold	93%
	SW2 OV Threshold	107%
	SW2 Current Limit	4.5 A
	SW2 Inductor	1 μ H
	SW2 Phase	225°
	SW2 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW2 WD Bypass	Regulator reacts upon a Watchdog
	SW2 OV Bypass	OV Protect Enabled
	SW2 UV Bypass	UV Protect Enabled
	SW2 ILIM Bypass	ILIM Fault Bypassed
SW3	SW3 Output Voltage	1.00000 V
	SW3 DVS Ramp	7.813/5.208 mV/ μ s
	SW3 UV Threshold	93%

Configuration report for PF8250-B OTP program ID: DB rev A

	SW3 OV Threshold	107%
	SW3 Current Limit	4.5 A
	SW3 Inductor	1 μ H
	SW3 Phase	0°
	SW3 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW3 WD Bypass	Regulator reacts upon a Watchdog
	SW3 OV Bypass	OV Protect Enabled
	SW3 UV Bypass	UV Protect Enabled
	SW3 ILIM Bypass	ILIM Fault Bypassed
SW4	SW4 Output Voltage	1.00000 V
	SW4 DVS Ramp	7.813/5.208 mV/ μ s
	SW4 UV Threshold	93%
	SW4 OV Threshold	107%
	SW4 Current Limit	4.5 A
	SW4 Inductor	1 μ H
	SW4 Phase	225°
	SW4 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW4 WD Bypass	Regulator reacts upon a Watchdog
	SW4 OV Bypass	OV Protect Enabled
	SW4 UV Bypass	UV Protect Enabled
	SW4 ILIM Bypass	ILIM Fault Bypassed
SW5	SW5 Output Voltage	1.10000 V
	SW5 DVS Ramp	7.813/5.208 mV/ μ s
	SW5 UV Threshold	93%

Configuration report for PF8250-B OTP program ID: DB rev A

	SW5 OV Threshold	107%
	SW5 Current Limit	4.5 A
	SW5 Inductor	1 μ H
	SW5 Phase	45°
	SW5 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW5 WD Bypass	Regulator reacts upon a Watchdog
	SW5 OV Bypass	OV Protect Enabled
	SW5 UV Bypass	UV Protect Enabled
	SW5 ILIM Bypass	ILIM Fault Bypassed
SW6	SW6 Output Voltage	1.10000 V
	SW6 DVS Ramp	7.813/5.208 mV/ μ s
	SW6 UV Threshold	93%
	SW6 OV Threshold	107%
	SW6 Current Limit	4.5 A
	SW6 Inductor	1 μ H
	SW6 Phase	270°
	SW6 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW6 WD Bypass	Regulator reacts upon a Watchdog
	SW6 OV Bypass	OV Protect Enabled
	SW6 UV Bypass	UV Protect Enabled
	SW6 ILIM Bypass	ILIM Fault Bypassed
SW7	SW7 Output Voltage	3.30 V
	SW7 UV Threshold	93%

Configuration report for PF8250-B OTP program ID: DB rev A

	SW7 OV Threshold	107%
	SW7 Current Limit	2.6 A
	SW7 Inductor	1 μ H
	SW7 Phase	180°
	SW7 PGOOD Control	Reg. is part of AND function to control PGOOD
	SW7 WD Bypass	Regulator reacts upon a Watchdog
	SW7 OV Bypass	OV Protect Enabled
	SW7 UV Bypass	UV Protect Enabled
	SW7 ILIM Bypass	ILIM Fault Bypassed

Table 6. LDO regulators

Functional block	Feature	OTP selection
LDO1	LDO1 Output Voltage	3.3 V
	LDO1 UV Threshold	93%
	LDO1 OV Threshold	107%
	LDO1 PGOOD Control	Reg. is part of AND function to control PGOOD
	LDO1 WD Bypass	Regulator reacts upon a Watchdog
	LDO1 Mode	Normal Mode
	LDO1 OV Bypass	OV Protect Enabled
	LDO1 UV Bypass	UV Protect Enabled
	LDO1 ILIM Bypass	ILIM Fault Bypassed
LDO2	LDO2 Output Voltage	3.3 V
	LDO2 UV Threshold	93%
	LDO2 OV Threshold	107%
	LDO2 PGOOD Control	Reg. is part of AND function to control PGOOD

Configuration report for PF8250-B OTP program ID: DB rev A

	LDO2 WD Bypass	Regulator reacts upon a Watchdog
	LDO2 Mode	Normal Mode
	LDO2EN Hardware Control	I2C Control Only
	VSELECT Hardware Control	LDO2 set by VSELECT. Low=3.3V / High=1.8V
	LDO2 OV Bypass	OV Protect Enabled
	LDO2 UV Bypass	UV Protect Enabled
	LDO2 ILIM Bypass	ILIM Fault Bypassed
LDO3	LDO3 Output Voltage	2.5 V
	LDO3 UV Threshold	93%
	LDO3 OV Threshold	107%
	LDO3 PGOOD Control	Reg. is part of AND function to control PGOOD
	LDO3 WD Bypass	Regulator reacts upon a Watchdog
	LDO3 Mode	Normal Mode
	LDO3 OV Bypass	OV Protect Enabled
	LDO3 UV Bypass	UV Protect Enabled
	LDO3 ILIM Bypass	ILIM Fault Bypassed
LDO4	LDO4 Output Voltage	3.3 V
	LDO4 UV Threshold	93%
	LDO4 OV Threshold	107%
	LDO4 PGOOD Control	Reg. is part of AND function to control PGOOD
	LDO4 WD Bypass	Regulator reacts upon a Watchdog
	LDO4 Mode	Normal Mode
	LDO4 OV Bypass	OV Protect Enabled
	LDO4 UV Bypass	UV Protect Enabled

Configuration report for PF8250-B OTP program ID: DB rev A

	LDO4 ILIM Bypass	ILIM Fault Bypassed
VSNVS	VSNVS Output Voltage	OFF

8 Legal information

8.1 Definitions

Draft - The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

8.2 Disclaimers

Limited warranty and liability - Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including -without limitation -lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Not with standing any damages that customer might incur for any reason whatsoever, NXP Semiconductors aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use - NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications - Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the

their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values - Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale - NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license - Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications - This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control - This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations - A non-English (translated) version of a document

8.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP - is a trademark of NXP B.V.

Contents

1 General description	1
2 Features and benefits	1
3 Applications	1
4 Ordering information	2
5 Power up sequence summary	2
6 Hardware configuration diagram	3
7 OTP configuration	4
8 Legal information	14

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2025 .

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 2025/6/13

Document identifier: R_MC33PF8250DBTS